cover story

Conquering 45nm Technology

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One step ahead and the trend continues...

Semiconductor industry has marked another milestone with successful release of 45nm Integrated Circuits. Now we have the world's smallest sized transistor based processor 'Penryn' from Intel, which is running well in their labs.
IBM, Chartered Semiconductor, Samsung and Infineon are already set for commercial production of 45nm CMOS technology in 2007.

Companies will start shipping manufactured chips with this technology from next year which is a fairer enough proof of conquering 45nm technology and by far, by large, a testimony for Gordan Moore's words.

Gordon Moore, co-founder of Intel Corporation has stated that "the implementation of high-k and metal materials marks the biggest change in transistor technology since the introduction of polysilicon MOS transistors in the late 1960s." You would think that was enough to brag about, but technology doesn't seems to stop here.

On 65 nanometre process, gate dielectric walls are 1.2 nanometre thick that's equivalent to five atomic layers across, if we put things into perspective. Now we have 45nm transistor with only 1.0nm gate dielectric walls.

This essentially means that engineers are designing chips on almost atomic structure level, and shrinking current silicon dioxide gate dielectric walls even further would exaggerate this even further.

The evolution of important parameters such as the integrated circuit (IC) complexity, the gate length, switching delay and supply voltage with a prospective vision down to the 22 nm CMOS technology continues. We really hope the *"Show must go on"*.

Table 1 gives an overview of the key parameters for technological nodes from 180 nm introduced in 1999, down to 22 nm, which is expected to be in production around 2011.

Technology node	**130 nm**	**90 nm**	**65 nm**	**45 nm**	**32 nm**	**22 nm**
First production	2001	2003	2005	2007	2009	2011
Effective gate length	70 nm	50 nm	35 nm	25 nm	17 nm	12 nm
Gate material	Poly SiO_2	Poly SiO_2	Poly SiON	Metal High K	Metal High K	Metal High K
Gate atoms	8	5	5	5-10	5-10	5-10
Kgates/mm^2	240	480	900	1500	2800	4500
Memory point (μ^2)	2.4	1.3	0.6	0.3	0.15	0.08

Table 1: Technological evolution and forecast up to 2011

The physical gate length is slightly smaller than the technological node. The gate material has long been polysilicon, with silicon dioxide (SiO_2) as the insulator between the gate and the channel (Fig. 1). The atom is a convenient measuring stick for the insulating material transistor beneath the gate. In 90 nm, the gate oxide was consisting of about five atomic layers, equivalent to 1.2 nm in thickness. The thinner the gate oxide, the higher the transistor current and consequently the switching speed. However, thinner gate oxide also means more leakage current. The ultimate limit seems to be 1.0 nm.

Starting with the 90nm technology, SiO_2 has been replaced by SiON dielectric, which features a higher permittivity and consequently improves the device performances while keeping the parasitic leakage current within reasonable limits. Starting with the 45-nm technology, leakage reduction has been achieved through the use of various high-K dielectrics such as Hafnium Oxide HfO2 (ε_r =12), Zyrconium Oxide ZrO_2 (ε_r =20), Tantalum Oxide Ta_2O_5 (ε_r =25) or Titanium Oxide TiO_2 (ε_r =40). This provides much higher device performance as if the device was fabricated in a technology using conventional SiO_2 with much reduced *"equivalent SiO_2 thickness"*.

The High-K dielectric enabled a thinner "equivalent" oxide thickness while keeping leakage current low. The "equivalent oxide thickness" TOXE is defined by Eq. 1. For the 45-nm technology, the high-K permittivity declared is 10 (Parameter "GateK"). The physical oxide thickness is 3.5 nm, and by applying Eq. 1, TOXE is 1.4nm. These parameters are in close agreement with those in general 45-nm gate stacks.

$$TOXE = \left(\frac{\varepsilon_{SiO2}}{\varepsilon_{high-k}} t_{high-k} \right) \quad \text{(Eq. 1)}$$

Where

ε_{SiO2} = Dielectric permittivity of SiO_2

ε_{high-k} = High-K dielectric permittivity

t_{high-k} = High-K oxide thickness (m)

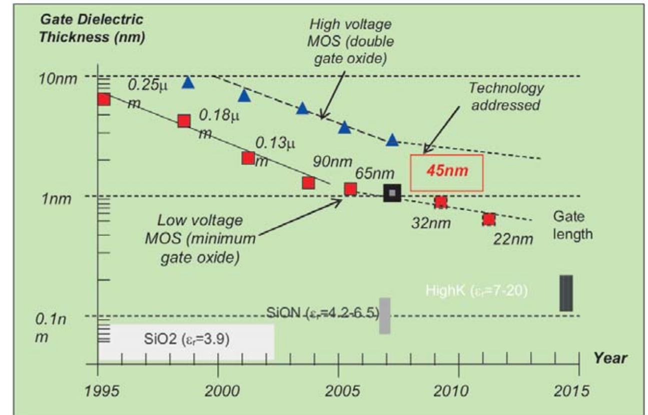


Figure 1 : The technology scale down towards nano-scale devices

In the 45-nm technology node, some IC manufacturers targeting low cost production have kept the polysilicon gate and the SiON oxide, while still achieving important speed and power improvements, thanks to channel length reduction. However, IC manufacturers oriented towards very high performances have replaced the SiON oxide by Hafnium Oxide to obtain an equivalent oxide thickness TOXE close to 1.0 nm.

At each lithography scaling, the linear dimensions are approximately reduced by a factor of 0.7, and the areas are reduced by factor of 2. Smaller cell sizes lead to higher integration density which has risen to nearly 2 million gates per mm^2 in the 45-nm technology.

The integrated circuit market has been growing steadily since many years, due to ever-increasing demand for electronic devices. The production of integrated circuits for various technologies over the years is illustrated in Fig. 2. It can be seen that a new technology has appeared regularly every two years, with a ramp up close to three years. The production peak is constantly increased, and similar trends should be observed for novel technologies such as 45nm (forecast peak in 2010).

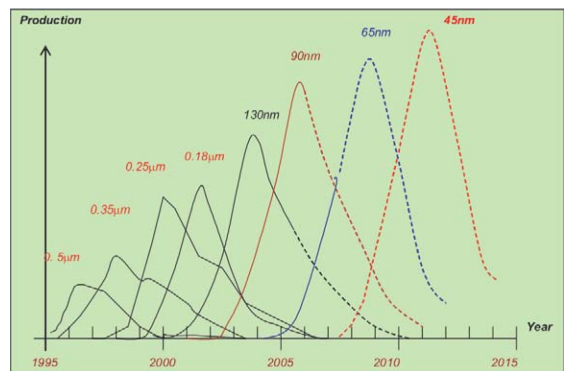


Figure 2 : Technology ramping every two years

Prototype 45-nm processes have been introduced by TSMC in 2004 and Fujitsu in 2005. In 2007, Intel announced its 45-nm

CMOS industrial process and revealed some key features about metal gates. The "Common Platform" including IBM, Chartered Semiconductor, Samsung and Infineon has set-up a 45-nm CMOS technology for commercial production in 2007. The transistor channels range from 25 nm to 40 nm in size (25 to 40 billionths of a meter). Some of the key features of the 45 nm technologies from various providers are given in Table 2.

Parameter	Value
V_{DD} (V)	0.85-1.2 V
Effective gate length (nm)	25-40
Ion N (μA/μm) at 1V	750-1000
Ion P (μA/μm) at 1V	350-530
Ioff N (nA/μm)	5-100
Ioff P (nA/μm)	5-100
Gate dielectric	SiON, HfO2
Equivalent oxide thickness (nm)	1.1-1.5
No. of metal layers	6-10
Interconnect layer permittivity K	2.2-2.6

Table 2: Key features of the 45nm technology

Compared to 65-nm technology, most 45-nm technologies offer:

- Θ 30 % increase in switching performance
- Θ 30 % less power consumption 2 times higher density
- Θ X 2 reduction of the leakage between source and drain and through the gate oxide

Gate Material

For 40 years, the SiO_2 gate oxide combined with polysilicon have been serving as the key enabling materials for scaling MOS devices down to the 90nm technology node. One of the struggles the IC manufacturers went through was being able to scale the gate dielectric thickness to match continuous requirements for improved switching performance. But the leakage current between drain/source and the gate became significant.

The combination of high dielectric materials with polysilicon gate has revealed unexpected increase of parasitic threshold voltage and severe degradation of the carrier mobility, which jeopardized the benefits of a scaled channel length. For the first time in 40 years of CMOS manufacturing, the poly gate has been abandoned. Nickel-Silicide (NiSi), Titanium-Nitride (TiN) etc. are the types of gate materials that provide acceptable threshold voltage and alleviate the mobility degradation problem (Fig. 3). It is interesting to note that most IC manufacturers do not reveal the exact structure of the metal gate. In combination with Hafnium Oxide (HfO_2,ε_r=12), the metal/high-k transistors feature outstanding current switching capabilities together with low leakage. Increased *on* current, decreased *off* current and significantly decreased gate leakage are obtained with this novel combination.

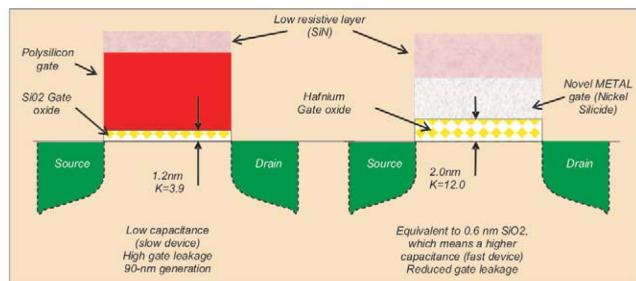


Figure 3: The metal gate combined with High-K oxide material enhance the MOS device performance in terms of switching speed and significantly reduce the leakage

The effective electron mobility is significantly reduced with a decrease of the equivalent gate oxide thickness, as seen in Fig. 4. It can be seen that the highest mobility is obtained with optimized TiN/HfO_2, while Poly/ HfO_2 do not lead to suitable performances.

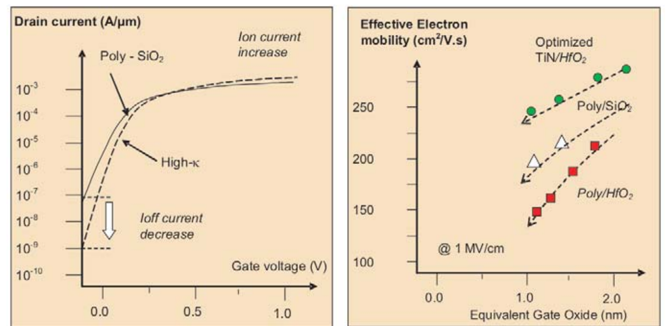


Figure 4: The metal gate combined with High-K oxide material enhances the Ion current and drastically reduces the Ioff current (left). Electron mobility vs. Equivalent gate oxide thickness for various materials (right)

Strained Silicon

Strained silicon has been introduced starting with the 90-nm technology, to speed-up the carrier mobility, which boosts both the n-channel and p-channel transistor performances. PMOS transistor channel strain has been enhanced by increasing the Germanium (Ge) content in the compressive SiGe (silicium-germanium) film. Both transistors employ ultra shallow source-drains to further increase the drive currents.

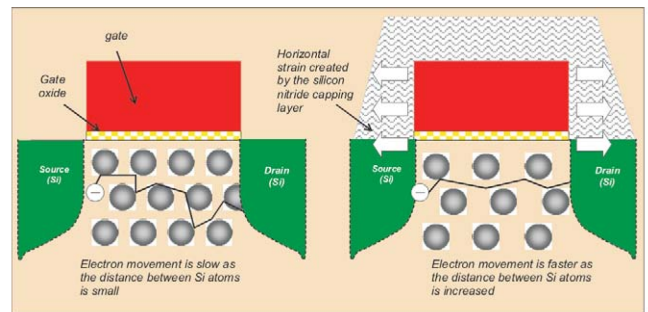


Figure 5: Tensile strain generated by a silicon-nitride capping layer which increases the distance between atoms underneath the gate, which speeds up the electron mobility of n-channel MOS devices

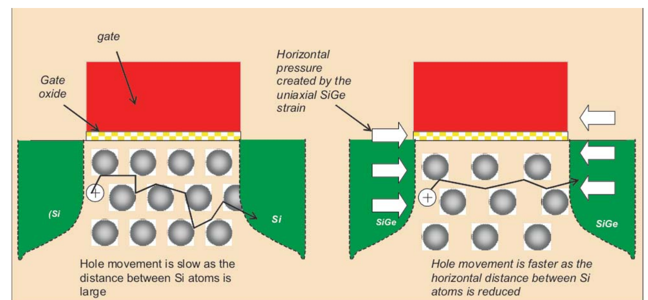


Figure 6: Compressive strain to reduce the distance between atoms underneath the gate, which speeds up the hole mobility of p-channel MOS devices

Let us assume that the silicon atoms form a regular lattice structure, inside which the carriers participating to the device current have to flow. In the case of electron carriers, stretching the lattice (by applying tensile strain) allows the electrons to flow faster from the source to the drain, as depicted in Fig. 5.

The mobility improvement exhibits a linear dependence with the tensile film thickness. An 80 nm film has resulted in a 10% saturation current improvement in Intel's 90nm technology. The strain may also be applied from the bottom with a uniform layer of an alloy of silicon and germanium (SiGe).
In a similar way, compressing the lattice slightly speeds up the p-type transistor, for which current carriers consist of holes (Fig. 6). The combination of reduced channel length, decreased oxide thickness and strained silicon achieves a substantial gain in drive

current for both nMOS and pMOS devices.

N-channel MOS device characteristics

The 45-nm technology uses a stack of high-k dielectric, metal (TiN) and polysilicon. Cross-sections of the n-channel MOS devices are given in Fig. 7. The nMOS gate is capped with a specific silicon nitride layer that induces lateral tensile channel strain for improved electron mobility.

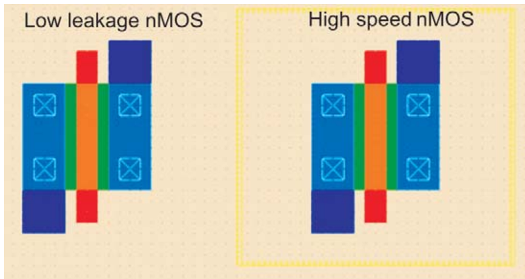


Figure 7.a: Low leakage & high speed versions of NMOS transistor

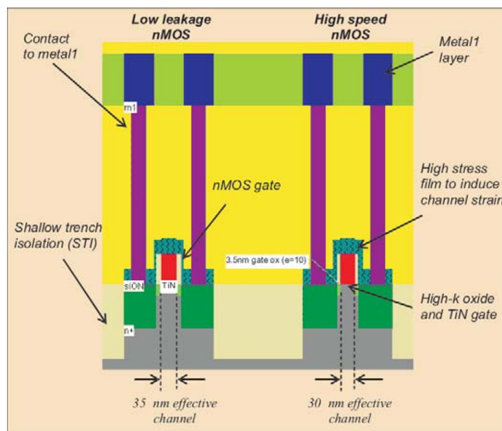


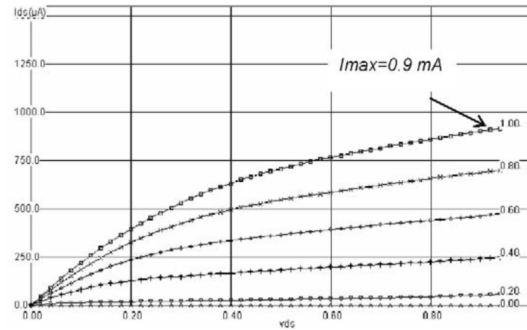
Figure 7.b: Cross-section of the nMOS devices

Parameter	NMOS Low leakage	NMOS High speed
Drawn length (nm)	40	40
Effective length (nm)	35	30
Threshold voltage (V)	0.20	0.18
Ion (mA/µm) at VDD=1.0V	0.9	1.2
Ioff (nA/µm)	7	200

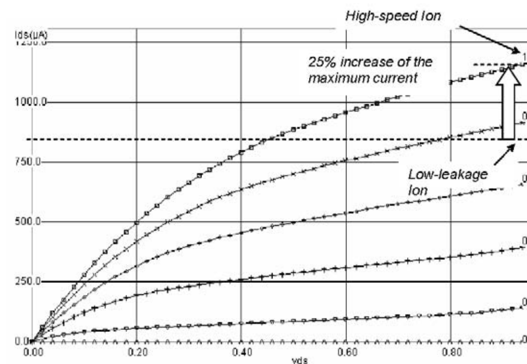
Table 3: nMOS parameters featured in the CMOS 45-nm technology

The device I/V characteristics of the low-leakage and high-speed MOS devices listed in Table 3 are obtained using the MOS model BSIM4. The cross-section of the low-leakage and high-speed MOS devices do not reveal any major difference (Fig. 7.b), except a reduction of the effective channel length. Concerning the low-leakage MOS, the I/V characteristics reported in Fig. 8 demonstrate a drive current capability of around 0.9 mA/µm for W=1.0 µm at a voltage supply of 1.0 V. For the high speed MOS devices do not reveal any major difference (Fig. 7.b), except a reduction of the effective channel length. Concerning the low-leakage MOS, the I/V characteristics reported in Fig. 8 demonstrate a drive current capability of around 0.9 mA/µm for W=1.0µm at a voltage supply of 1.0 V. For the high speed MOS, the effective channel length is slightly reduced as well as the threshold voltage, to achieve a drive current around 1.2 mA/µm.

The drawback of the high-speed MOS current drive is the leakage current which rises from 7 nA/µm (low leakage) to 200 nA/µm (high speed), as seen in the Id/Vg curve at the X axis location corresponding to Vg= 0 V (Fig. 9-b).

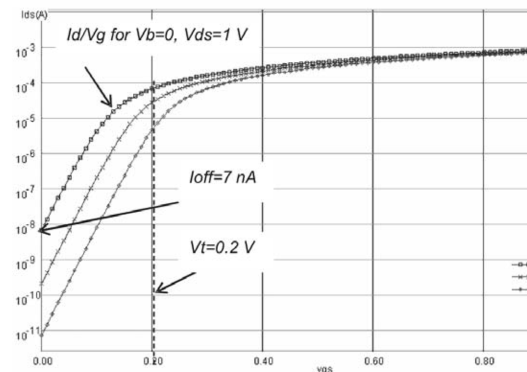


(a) Low leakage W=1µm, Leff= 35nm

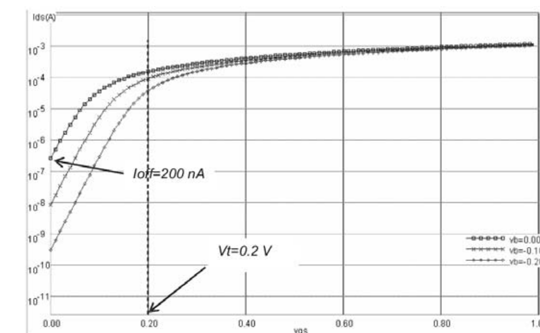


(b) High speed W=1µm, Leff= 30nm

Figure 8: Id/Vd characteristics of the low leakage and high speed nMOS devices



(a) low leakage MOS (Leff=35 nm)



(b) high speed MOS (W=1 µm, Leff=30 nm)

Figure 9: Id/Vg characteristics (log scale) of the low leakage and high-speed nMOS devices

P-channel MOS device characteristics

The PMOS drive current in this 45-nm technology is around 550 µA/µm for the low-leakage MOS and up to 700 µA/µm for the high-speed MOS. These values (see Table 4) are not particularly high, as the target applications for this technology are low-power embedded electronics, in contrast with 45-nm technology targeted to ultra high-speed microprocessors (see Fig. 11 for an illustration of 45-nm technology variants). The leakage current is remarkably low, around 5 nA/µm for the low-leakage MOS and near 180 nA/µm for the high-speed device. The cross-section of the pMOS device reveals an SiGe material that induces compressive strain to obtain maximum current capabilities (Fig. 10).

Parameter	pMOS Low leakage	pMOS High speed
Drawn length (nm)	40	40
Effective length (nm)	35	30
Threshold Voltage (V)	0.19	0.17
Ion (mA/µm) at VDD=1.0V	0.55	0.70
Ioff (nA/µm)	5	180

Table 4: pMOS parameters featured by the 45-nm CMOS technology

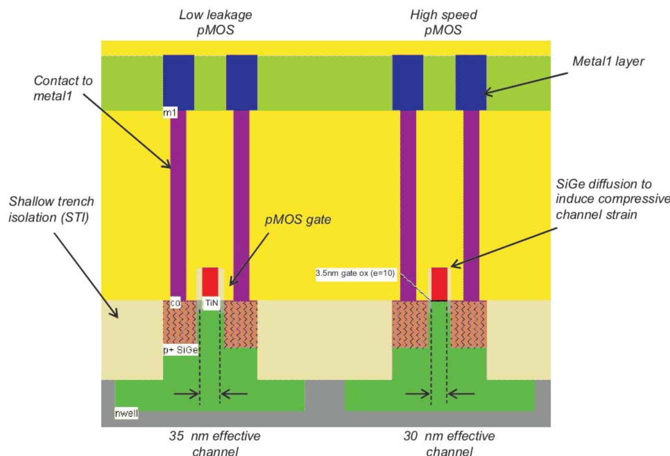


Figure 10: Cross-section of the pMOS devices

45-nm process variants

There may exist several variants of the 45-nm process technology. One corresponds to the highest possible speed, at the price of a very high leakage current. This technology is called "High speed" as it is dedicated to applications for which the highest speed is the primary objective: fast microprocessors, fast DSP, etc.

The second technological option called "General Purpose" (Fig. 11) is targeted to standard products where the speed factor is not critical. The leakage current is one order of magnitude lower than for the high-speed variant, with gate switching decreased by 50%. Only this technology has been implemented in Microwind.

There may also exist a third variant called low leakage (bottom left of Fig. 11). This variant concerns integrated circuits for which the leakage current must remain as low as possible, a criterion that ranks first in applications such as embedded devices, mobile phones or personal organizers. The operational voltage is usually from 0.8 V to 1.2 V, depending on the technology variant. In Microwind, we decided to fix VDD at 1.0 V in the cmos45nm.RUL rule file, which represents a compromise between all possible technology variations available for this 45-nm node.

MOS Types

At least three types of MOS devices exist within the "General Purpose" variant of the 45-nm technology implemented in Microwind, which may be confusing as they partially reuse the technology terminology: the low-leakage MOS is the default MOS device, and the high-speed MOS has higher switching performance but higher leakage. The third MOS option is the high voltage MOS used for input/output interfacing. In Microwind's cmos45nm rule file, the I/O supply is 1.8 V. Most foundries also propose 2.5 V and 3.3 V interfacing.

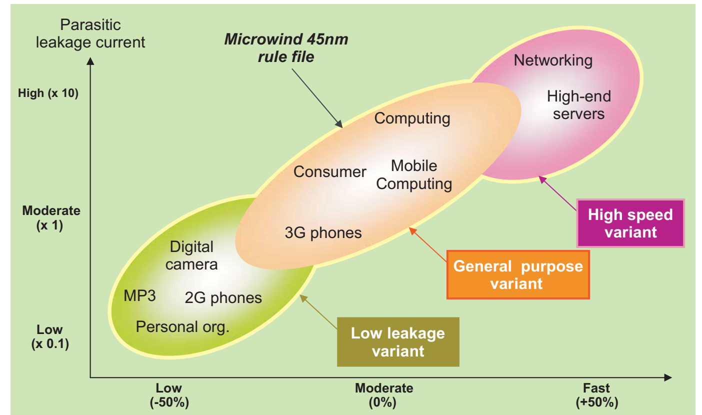


Figure 11 : Introducing three variants of the 45-nm technology

The main objective of the low leakage MOS is to reduce the *Ioff* current significantly, that is the small current that flows between drain and source with a zero gate voltage. The price to pay is a reduced *Ion* current. The designer has the choice of using high-speed MOS devices, which have high *Ioff* leakages but large *Ion* drive currents.

The Future

45nm process technology extends 15-year record of ramping production on a new process generation every two years and demonstrates the ability to continue delivering the benefits of Moore's Law.

In 2005, researchers from Intel and QinetiQ jointly developed prototype transistors with Indium Antimonide (InSb is a III-V compound semiconductor), which show promise for future high-speed and yet very-low-power logic applications. These transistors could be used in Intel's logic products in the second half of the next decade and could be a factor in the continuation of Moore's Law well beyond 2015.

We need to wait until 2007 year end to come face to face with Intel's Penryn and AMD's K8L 45nm technology based Processor series.

Many fabrication labs are also well along in developing next two process generations, 32nm and 22nm, due in 2009 and 2011, respectively.